MAP report

Release 14.7 Map P.20131013 (nt64)

Xilinx Mapping Report File for Design 'WS'

Design Information

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Command Line : map -intstyle ise -p xa7a100t-csg324-2I -w -logic\_opt off -ol

high -t 1 -xt 0 -register\_duplication off -r 4 -mt off -ir off -pr off -lc off

-power off -o WS\_map.ncd WS.ngd WS.pcf

Target Device : xa7a100t

Target Package : csg324

Target Speed : -2i

Mapper Version : aartix7 -- $Revision: 1.55 $

Mapped Date : Sun Jul 10 19:49:19 2022

Design Summary

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Number of errors: 0

Number of warnings: 23

Slice Logic Utilization:

Number of Slice Registers: 1 out of 126,800 1%

Number used as Flip Flops: 0

Number used as Latches: 1

Number used as Latch-thrus: 0

Number used as AND/OR logics: 0

Number of Slice LUTs: 2 out of 63,400 1%

Number used as logic: 2 out of 63,400 1%

Number using O6 output only: 2

Number using O5 output only: 0

Number using O5 and O6: 0

Number used as ROM: 0

Number used as Memory: 0 out of 19,000 0%

Number used exclusively as route-thrus: 0

Slice Logic Distribution:

Number of occupied Slices: 1 out of 15,850 1%

Number of LUT Flip Flop pairs used: 2

Number with an unused Flip Flop: 1 out of 2 50%

Number with an unused LUT: 0 out of 2 0%

Number of fully used LUT-FF pairs: 1 out of 2 50%

Number of unique control sets: 1

Number of slice register sites lost

to control set restrictions: 7 out of 126,800 1%

A LUT Flip Flop pair for this architecture represents one LUT paired with

one Flip Flop within a slice. A control set is a unique combination of

clock, reset, set, and enable signals for a registered element.

The Slice Logic Distribution report is not meaningful if the design is

over-mapped for a non-slice resource or if Placement fails.

OVERMAPPING of BRAM resources should be ignored if the design is

over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:

Number of bonded IOBs: 21 out of 210 10%

Specific Feature Utilization:

Number of RAMB36E1/FIFO36E1s: 0 out of 135 0%

Number of RAMB18E1/FIFO18E1s: 0 out of 270 0%

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

Number used as BUFGs: 1

Number used as BUFGCTRLs: 0

Number of IDELAYE2/IDELAYE2\_FINEDELAYs: 0 out of 300 0%

Number of ILOGICE2/ILOGICE3/ISERDESE2s: 0 out of 300 0%

Number of ODELAYE2/ODELAYE2\_FINEDELAYs: 0

Number of OLOGICE2/OLOGICE3/OSERDESE2s: 0 out of 300 0%

Number of PHASER\_IN/PHASER\_IN\_PHYs: 0 out of 24 0%

Number of PHASER\_OUT/PHASER\_OUT\_PHYs: 0 out of 24 0%

Number of BSCANs: 0 out of 4 0%

Number of BUFHCEs: 0 out of 96 0%

Number of BUFRs: 0 out of 24 0%

Number of CAPTUREs: 0 out of 1 0%

Number of DNA\_PORTs: 0 out of 1 0%

Number of DSP48E1s: 0 out of 240 0%

Number of EFUSE\_USRs: 0 out of 1 0%

Number of FRAME\_ECCs: 0 out of 1 0%

Number of IBUFDS\_GTE2s: 0 out of 4 0%

Number of ICAPs: 0 out of 2 0%

Number of IDELAYCTRLs: 0 out of 6 0%

Number of IN\_FIFOs: 0 out of 24 0%

Number of MMCME2\_ADVs: 0 out of 6 0%

Number of OUT\_FIFOs: 0 out of 24 0%

Number of PCIE\_2\_1s: 0 out of 1 0%

Number of PHASER\_REFs: 0 out of 6 0%

Number of PHY\_CONTROLs: 0 out of 6 0%

Number of PLLE2\_ADVs: 0 out of 6 0%

Number of STARTUPs: 0 out of 1 0%

Number of XADCs: 0 out of 1 0%

Average Fanout of Non-Clock Nets: 2.67

Peak Memory Usage: 4994 MB

Total REAL time to MAP completion: 16 secs

Total CPU time to MAP completion: 16 secs

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Section 1 - Errors

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Section 2 - Warnings

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WARNING:LIT:701 - PAD symbol "clock" has an undefined IOSTANDARD.

WARNING:LIT:702 - PAD symbol "clock" is not constrained (LOC) to a specific

location.

WARNING:PhysDesignRules:2452 - The IOB myState<1> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB moist<0> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB moist<1> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB moist<2> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB mySeg<0> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB mySeg<1> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB tempOut is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB mySeg<2> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB mySeg<3> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB mySeg<4> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB lightOut is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB mySeg<5> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB mySeg<6> is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB temp is either not constrained (LOC) to a

specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB clock is either not constrained (LOC) to

a specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB light is either not constrained (LOC) to

a specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB reset is either not constrained (LOC) to

a specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB moistOut<0> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB moistOut<1> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB moistOut<2> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB myState<0> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

Section 3 - Informational

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INFO:LIT:244 - All of the single ended outputs in this design are using slew

rate limited output drivers. The delay on speed critical single ended outputs

can be dramatically reduced by designating them as fast outputs.

INFO:Pack:1716 - Initializing temperature to 100.000 Celsius. (default - Range:

-40.000 to 100.000 Celsius)

INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to

1.050 Volts)

INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report

(.mrp).

INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary

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2 block(s) optimized away

Section 5 - Removed Logic

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Optimized Block(s):

TYPE BLOCK

GND XST\_GND

VCC XST\_VCC

Section 6 - IOB Properties

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| IOB Name | Type | Direction | IO Standard | Diff | Drive | Slew | Reg (s) | Resistor | IOB |

| | | | | Term | Strength | Rate | | | Delay |

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| clock | IOB | INPUT | LVCMOS18 | | | | | | |

| light | IOB | INPUT | LVCMOS18 | | | | | | |

| lightOut | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| moist<0> | IOB | INPUT | LVCMOS18 | | | | | | |

| moist<1> | IOB | INPUT | LVCMOS18 | | | | | | |

| moist<2> | IOB | INPUT | LVCMOS18 | | | | | | |

| moistOut<0> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| moistOut<1> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| moistOut<2> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| mySeg<0> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| mySeg<1> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| mySeg<2> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| mySeg<3> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| mySeg<4> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| mySeg<5> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| mySeg<6> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| myState<0> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| myState<1> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| reset | IOB | INPUT | LVCMOS18 | | | | | | |

| temp | IOB | INPUT | LVCMOS18 | | | | | | |

| tempOut | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

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Section 7 - RPMs

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Section 8 - Guide Report

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Guide not run on this design.

Section 9 - Area Group and Partition Summary

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Partition Implementation Status

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No Partitions were found in this design.

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Area Group Information

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No area groups were found in this design.

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Section 10 - Timing Report

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A logic-level (pre-route) timing report can be generated by using Xilinx static

timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the

mapped NCD and PCF files. Please note that this timing report will be generated

using estimated delay information. For accurate numbers, please generate a

timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing

Analyzer Reference Manual; for more information about TRCE, consult the Xilinx

Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

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Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

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Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

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Use the "-detail" map option to print out the Utilization by Hierarchy section.